REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 remain in the application. Claim 1 has been amended.

Claim 1 has been amended to further recite features relating to the type of data stored in the memory device and that the method according to the present invention provides additional information about the stored data bits, as described on page 9, line 13 to page 10, line 10 of the instant specification.

More specifically, the original data is reconstructed from the stored data taking into account the additional information.

In item 2 on page 2 of the final Office Action dated April 8, 2004, claims 1-4 have been rejected as being anticipated by Iida (U.S. Patent 4,748,594) under 35 U.S.C. § 102(b).

Iida discloses an integrated circuit device having a memory. A plurality of identical versions, that is, different sets, of a given piece of data are stored at different addresses in the memory 200. The information is read out on a time-division basis. When the three sets of information have been read out

a logic operation is performed in the majority circuit so that an output is obtained according to the truth table shown in Table 1 (col. 5) of Iida. The integrated circuit as described by Iida (see col. 3, line 10), has original data being reconstructed by using "means for performing a majority logic operation." In contrast, the present claimed invention allows the original data to be reconstructed by comparing the reconstructed data with the data stored in the memory device, taking into account the additional information that is stored as further described on in page 9, line 13 to page 10, line 10 and page 11, line 14 to page 12, line 5 of the instant specification. This feature clearly is different from the method disclosed by Iida. Iida does not disclose or teach reconstructing the originally stored data from the **data stored a plurality of times by taking into account the additional information about whether it is more likely that the stored data bits will change their level from 0 to 1 or from 1 to 0.**

The Examiner has referred to col. 3, line 10 as providing the basis in Iida for the claim limitation "reconstructing the originally stored data...from the data stored...and the additional information dependent on the data stored in the memory device." However, Iida discloses "...temporarily storing the earlier read-out information...performing a majority logic operation on the sets of read-out information,

and...taking out correct information from the majority logic...." There is no disclosure of reconstructing the originally stored data taking into account the "additional information" as recited in the claim 1 of the instant application.

Clearly, Iida does not show "providing a memory device for storing data bits that may change their level from 0 to 1 or from 1 to 0, it being more likely that the stored data bits will change their level from 0 to 1 than from 1 to 0, or vice versa", "providing additional information about whether it is more likely that the stored data bits will change their level from 0 to 1 or from 1 to 0", and "reconstructing the originally stored data as required from the data stored a plurality of times, taking into account the additional information" as recited in claim 1 of the instant application.

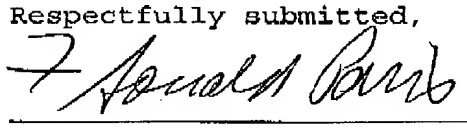
It is accordingly believed to be clear that Iida, whether taken alone or in any combination, does not show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-4 are solicited.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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FDP/bb

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